Loren Ashfield

Computer Engineer at UCSB

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About

I am a rising senior majoring in Computer Engineering at UC Santa Barbara, with a passion for understanding computers from the ground up. My interests lie at the intersection of VLSI design, computer architecture, and emerging materials, and I am excited by opportunities that combine system-level design with low-level optimization. I am proficient with industry-standard tools such as Cadence, SPICE, and Verilog, and have hands-on experience in digital and analog circuit simulation, verification, and design. Beyond hardware, I also have experience developing full-stack, end-to-end software solutions and applying AI and machine learning models to real-world industrial problems.

Education

UC Santa Barbara — Santa Barbara, CA
BS, Computer Engineering — 2022 - 2026

Newark Academy — Livingston, NJ
High School Diploma — 2018 - 2022

Experience

Student Researcher — UCSB Nanoelectronics Research Lab — 04/2025 - Present

- Exploring the possibility of fabricating ULTRARAM, a novel memory concept built on III-V materials, on wafers utilizing 2D material substrates.

Lab Systems Engineer — Yonder Materials — 08/2024 - Present

- Creating full-stack software applications to power AI-driven, high-throughput materials discovery.
- Working in lab alongside chemistry team, engaging hands on with deliverables and shadowing experienced material researchers.
- Designing custom PCBs to allow software to work with high-throughput electrochemistry setup.

ECE Tutor — UC Santa Barbara — 02/2025 - 06/2025

- Working for MESA University Program at UCSB providing one on one tutoring for first-generation and low-income students.
- Tutoring Digital Design Principles (ECE 152A) and Sensor and Peripheral Interface Design (ECE 153B)

Embedded Systems Research Assistant — Universidad Carlos III de Madrid — 06/2024 - 07/2024

- Evaluated the effects of random bit changes on consumer grade microprocessors to determine reliability in New Space applications.
- Wrote low footprint benchmarks for ARM Cortex-M and RISC-V embedded processors using explicit register management, testing with and without operating systems.
- Prepared the benchmark for irradiation campaigns controlled by an external host, sending data over serial communication to catalog misbehaviors.

Projects

32kb SRAM — 12/2024

- Designed 32kb SRAM from scratch on Cadence Virtuoso on a 130nm process node.
- Built all necessary circuits to power SRAM array, including precharge circuitry, sense amps, decoders, and more.
- Ran SPICE tests to verify and benchmark SRAM performance, corroborated by hand calculations.

Societies and Honors

Dean's Honors, UCSB, Earned every quarter since matriculation — 2022 - Present
Tau Beta Pi, Member of national engineering honor society — 2024 - Present

Alpha Tau Omega, Served one year as social chair, coordinating large scale trips and events 2022 - Present

Skills

Programming Languages: Python, C/C++, Assembly, Java, JavaScript, CSS, HTML
Tools and Frameworks: Cadence, LTspice, ModelSim, Quartus, SUE Design Manager, NST (New SPICE Tool), Git, Verilog, SystemVerilog, VHDL, Conda, PyTorch, Linux, Streamlit, PyQT, Docker, Poetry, Markdown
Languages: English